

CS 315-01 RISC-V Emulation Dev

Project 04 out today

Project 03 exam problems

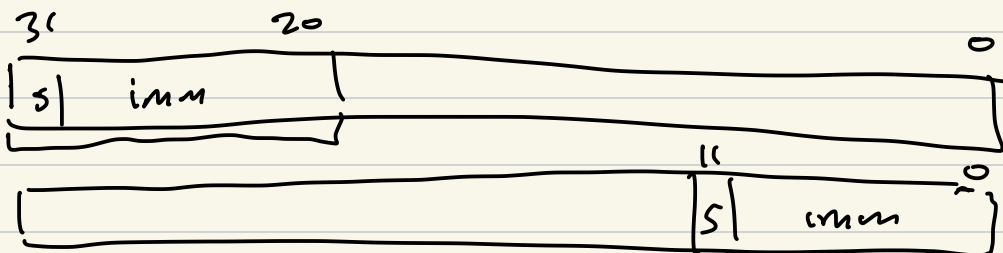
OH today 12pm to 2:30pm

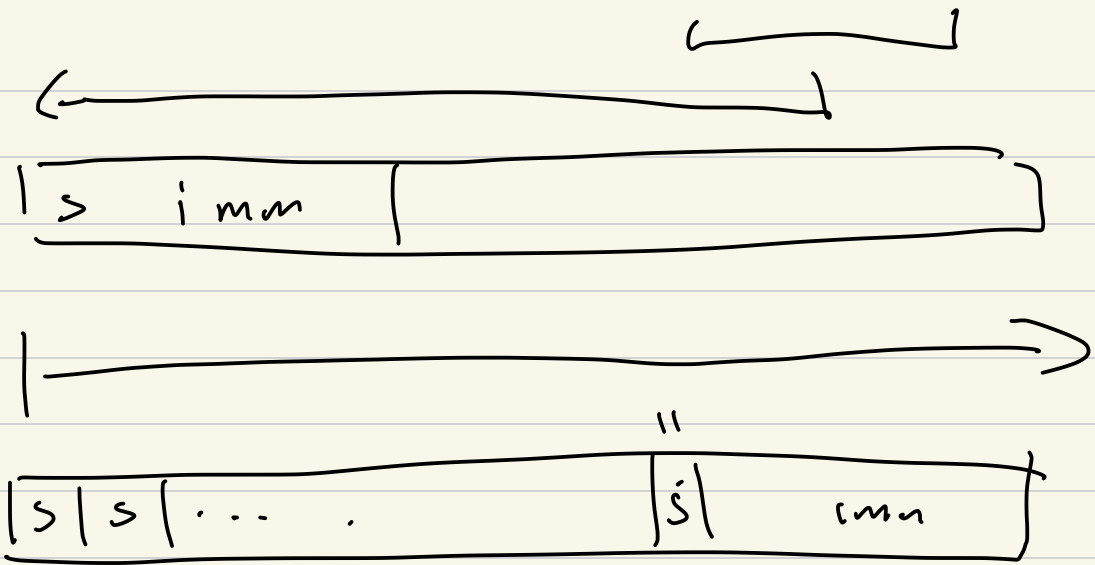
rv_emu.c given 97]
rv_emu.c sol 203]

li a0, 99 ←

0x06300813

0000 0110 0011 0000 0000 0101 0001 0011
 f3 rd ↑
 000 opcode





Branches

Extract fields

$$\left[\begin{array}{l} \text{funct} \\ \text{rs1} \\ \text{rs2} \end{array} \right]$$
 imm

branch immediate

- 1) get parts
- 2) combine parts
- 3) sign extend

1) get parts

`uint32_t imm_12 = get_bits(iw, 31, 1);`

`uint32_t imm_11 = get_bits(iw, 7, 1);`

`uint32_t imm_10_5 = get_bits(iw, 25, 6);`

`uint32_t imm_4_1 = get_bits(iw, 8, 4);`

2) combine parts

`uint64_t immu;`

`immu = (imm_12 << 12) | (imm_11 << 11)`

`→ | (imm_10_5 << 5) | (imm_4_1 << 1) | 0`

3) sign extend

`int64_t imm = sign_extend(immu, 12);`

Loads and Stores

lw a0, offset(a1)

$$a0 = *a1$$

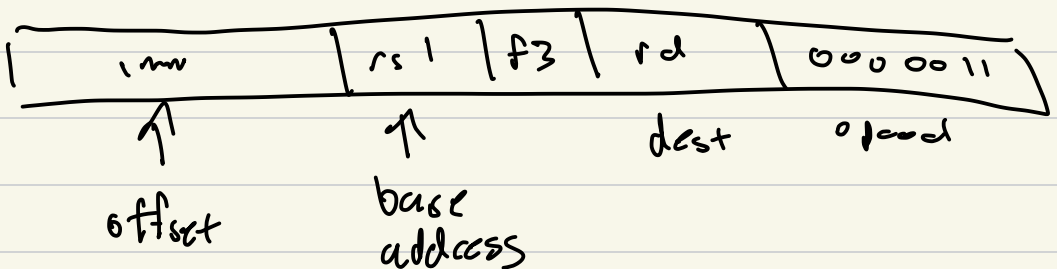
uint32_t a0;

$$a0 = *((\text{uint32}_t *) a1)^;$$

target address (TA)

$$TA = a1 + \text{offset}$$

$$rd = *((\text{uint32}_t *) TA);$$



lb	$\text{uint8}_t *$
lw	$\text{uint32}_t *$
ld	$\text{uint64}_t *$

Store

SW a0, offset(a1)

TA = a1 * offset

* (uint32_t*) TA) = a0 ;